



# PowerWise™ Interface Specification

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**ARM**

 **National**  
*Semiconductor*  
The Sight & Sound of Information

## Revision History

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# 1 Acronyms and Terms

AVS	Adaptive Voltage Scaling
DVS	Dynamic Voltage Scaling
ENABLE	External enable signal
IC	Integrated Circuit
I/O	Input/Output
LSB	Least Significant Bit
MSB	Most Significant Bit
PC	Power Controller
PLL	Phase-Locked Loop
PMIC	Power Management Integrated Circuit
PWROK	Power OK indicator
PWI	PowerWise Interface
RESETN	External reset signal
SPWI	Serial PWI-interface data line
SCLK	Serial PWI-interface clock line
SoC	System-on-a-Chip

## 2 Introduction

### 2.1 Background and Scope of PWI

The complexity and performance requirements of mobile phones and other portable electronic devices are increasing at an ever-accelerating rate. As the demand for new high performance, high data rate features is increasing, system level power management is becoming very critical. The use of advanced power management techniques to reduce power consumption and improve battery life is becoming more important than ever before.

Reducing power consumption of digital processors in portable electronic devices can improve the battery life and increase the available power budget for features such as color screens and backlights, which are becoming standard features on portable devices such as wireless handsets, handheld gaming consoles and portable media players.

To minimize power consumption of digital processors in portable electronic devices, system and IC designers have started to use advanced power management techniques. Advanced hardware and software techniques are now being used to accurately monitor and control processor performance level required for a given workload or application. Advanced techniques are also being used to control various supply voltages based on the performance level. Rapid deployment of such advanced power management techniques requires interface standardization. This PowerWise Interface (PWI) specification addresses hardware interface standardization.

The scope of PWI is limited to the interface that can be used to monitor and control various processor voltages such as supply voltage, threshold voltages, etc. The interface is intended to support advanced power management techniques.

### 2.2 Overview

The PowerWise Interface is a 2-wire serial interface, connecting the integrated Power Controller (PC) of a SoC (System on Chip) processor system with a PMIC (Power Management Integrated Circuit) voltage regulation system that allows system designers to dynamically adjust the supply and threshold voltages on digital processors. Within the PC, the PWI related functions are referred to as the "master". Within the PMIC, the PWI related functions are referred to as the "slave." The PWI specification defines the operating states, the register set, the command set, the physical interface, and the protocol for data communication between the PWI master and the PWI slave to insure the compatibility of command and data exchanges. The PWI command set includes slave operating state control, register read, register write, and voltage adjust commands. The specification provides provision for user defined registers in the PWI slave.

While references are made herein to advanced power management techniques such as Dynamic Voltage Scaling (DVS), Adaptive Voltage Scaling (AVS), Dynamic Body Biasing (DBB), or Dynamic Threshold Scaling (DTS), Adaptive Body Biasing (ABB), or Adaptive Threshold Scaling (ATS), etc., this PowerWise Interface Specification specifies only the interconnections and signaling required for interoperability and specifically excludes any implementations of such techniques.

### 2.3 Intended Audience

This document is intended for developers of PowerWise compliant products.

## 3 System Architecture

### 3.1 Power Management Concept

Power consumption in a digital processor is a combination of active and static power consumption.

To reduce total power consumption of a processor, the PowerWise interface can be used in conjunction with external, compliant PMIC products to realize advanced power management techniques such as Dynamic Voltage Scaling (DVS), Adaptive Voltage Scaling (AVS), Dynamic Body Biasing (DBB), or Dynamic Threshold Scaling (DTS), Adaptive Body Biasing (ABB), or Adaptive Threshold Scaling (ATS), etc. Implementations of these techniques form no part of this specification and may be subject to licensing restrictions.

### 3.2 System Overview

The minimum system configuration consists of a SoC with a PowerWise Interface master (PWI master), a PMIC with a PowerWise Interface slave (PWI slave), and the 2-wire PowerWise interface connecting the PWI master and PWI slave. See figure 3-1.

The PMIC supplies various voltages to the SoC. The voltage levels provided by the PMIC can be adjusted with commands sent from the PWI master to the PWI slave. The PMIC must contain a core voltage regulator. The PMIC can also include a separate memory supply voltage regulator (including support for memory retention voltage), I/O supply voltage regulator and a fixed voltage regulator used by PLLs, oscillators and various housekeeping functions needed on the SoC. The PowerWise interface includes provisions to control the output voltages of other voltage regulators such as transistor body biasing voltages. It is not mandatory to have these functions implemented in the PMIC with control via the PWI.

The PMIC contains two external control signals: RESETN and ENABLE. These signals are used to implement power on/off control and PMIC state sequencing when the PWI master is not active.

A PWI compliant system may be comprised of a single PMIC or combination of discrete voltage regulators and other analog and mixed signal components. The PMIC can include other integrated functions in addition to the PWI features and functions described in this specification.

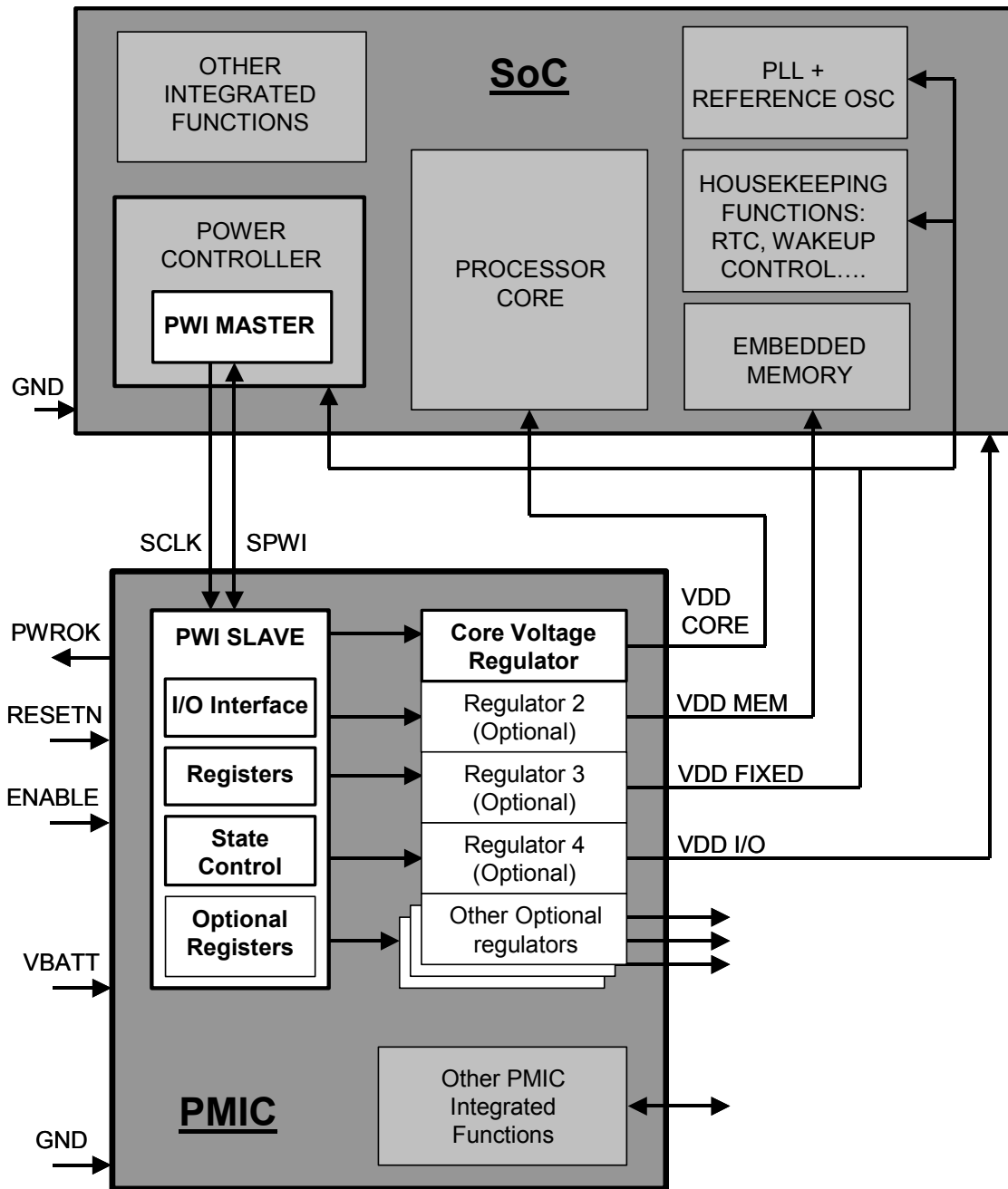
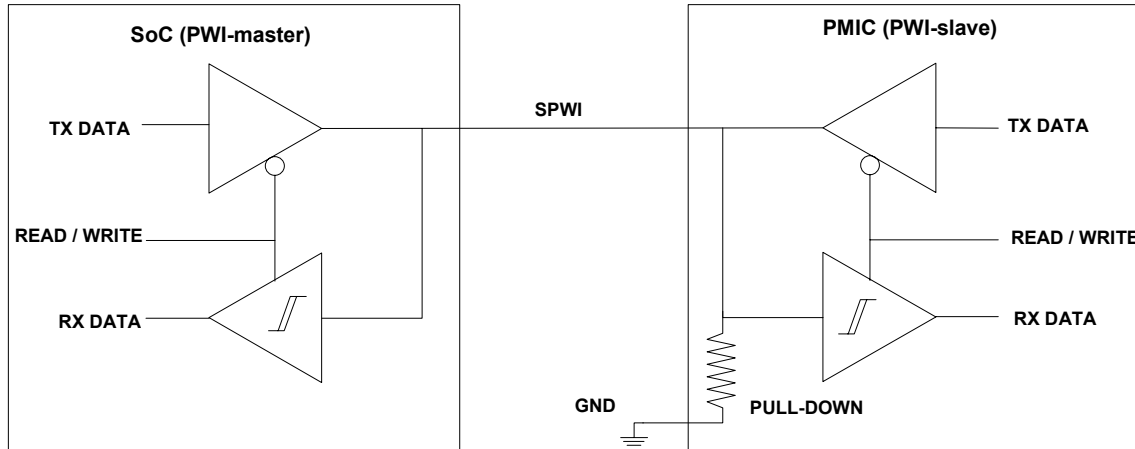


Figure 3-1. PowerWise System Diagram

## 4 Physical Interface

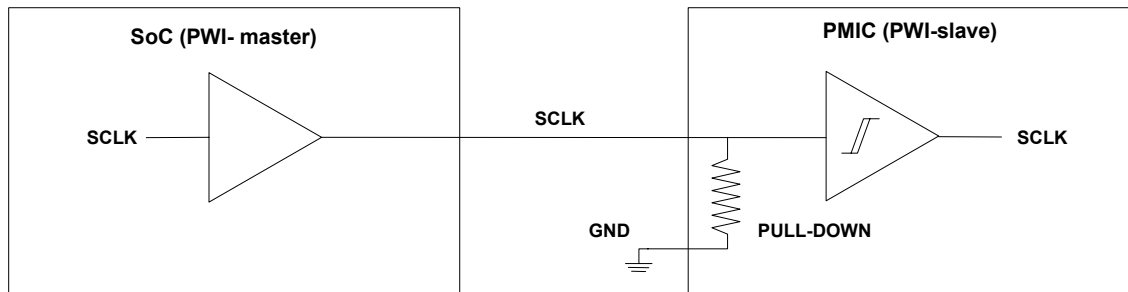
### 4.1 I/O Structures

The PWI is a two-wire interface with one serial bi-directional data line (SPWI) and one clock line (SCLK) controlled by the PWI master. The following figure shows the I/O structures required for the data line for both master and slave.



**Figure 4-1. SPWI Master and Slave I/O Cells**

The following figure shows the same information for the clock line (SCLK).



**Figure 4-2. SCLK Master and Slave I/O Cells**

It is possible, and permissible, to implement the pull-down resistors using external components instead of integrated resistors. The pull-down should be in the range 0.5M to 2M ohms.

The I/O cells should be implemented with high impedance input structures and output drivers that are high impedance when not active. I/O cells with typical CMOS structures will normally provide these characteristics. The total connected load on SCLK and SPWI, including package and circuit board capacitance, should be limited to 15pf.

## 4.2 IO Voltage and Logic Levels

The I/O supply voltage ( $V_{I/O}$ ) level is defined by the requirements of the SoC circuit. PWI slave SPWI driver should operate from the same voltage level as the PWI master. This prevents the possibility of damage due to over voltage to the SoC. Level shifting functions on the PWI slave are handled before the slave SPWI driver.

The PWI logic levels are defined in relation to the I/O voltage used on the interface. The I/O voltage is technology and design dependent. The voltage levels specified in the appropriate EIA/JEDEC standard apply both to the PWI interface signals and to any external control and status signals (ENABLE, RESETN and PWROK).

## 4.3 PWI Clock (SCLK)

The PWI master drives the PWI clock line. Although a pull-down resistor is connected between the SCLK and GND-voltage on the slave, the PWI master drives the clock signal actively high and low (CMOS inverter type driver stage).

The SCLK frequency range is 0 MHz – 15 MHz. The clock runs only when data is being transferred. Otherwise the SCLK signal line is at logic low voltage. Minimum pulse width ( $T_P$ ) of the clock signal is 26 ns.

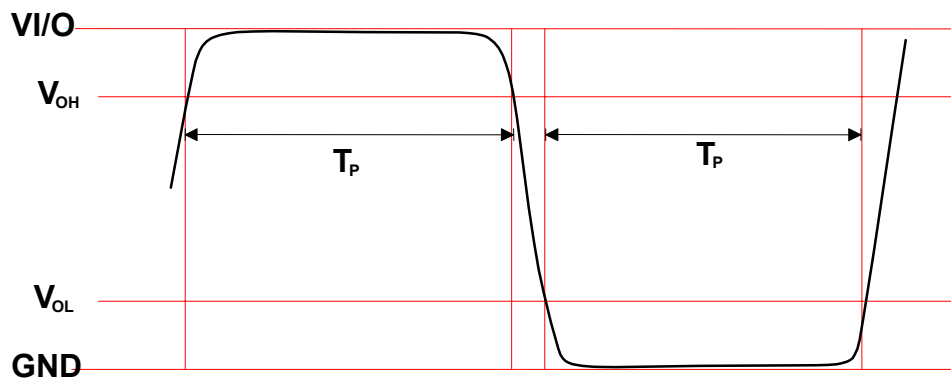


Figure 4-3. SCLK Timing Specification (clock running)

## 4.4 PWI Data-line (SPWI)

The PWI data-line is bi-directional. Data is written on the falling edge of the SCLK and read on the rising edge of the SCLK.

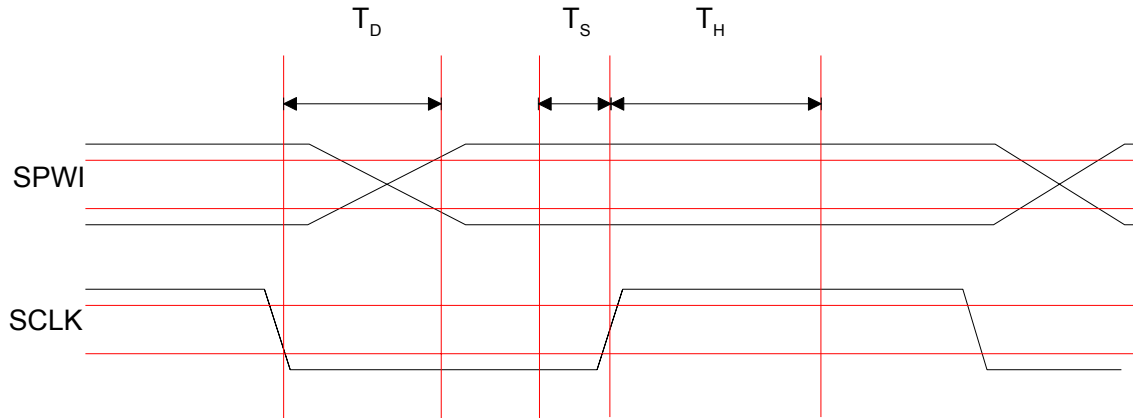


Figure 4-4. PWI Timing

Table 4-1. Timing Parameters

Symbol	Description	Value	Constraint type
$T_D$	Data valid time	18 ns	Maximum
$T_S$	Setup time	5 ns	Minimum
$T_H$	Hold time	10 ns	Minimum

Timing is referenced to the VOH and VOL levels of the appropriate EIA/JEDEC standard.

## 4.5 Control and Status Signals

The PWI compliant PMIC has three I/O signals in addition to the SCLK and SPWI signals. These are RESETN, ENABLE, and power OK indicator PWROK. ENABLE and RESETN are asynchronous inputs, and PWROK is an asynchronous output.

The ENABLE and RESETN signals are used to control the power-up sequence of the PMIC when PWI master does not yet have power and to connect the PMIC with the Power Up / Power Down control system of the application.

Alternate configuration: If the PMIC contains integrated control circuitry to correctly sequence and manage the PWI operating states described in section 7 then the ENABLE and RESETN signals are not required as external product pins.

Refer to section 7 for a detailed description of the operating states and the usage of these signals.

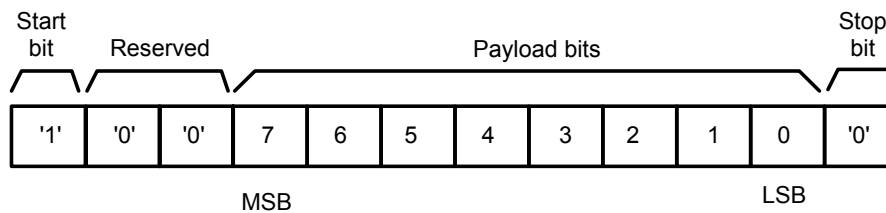
## 5 Protocol

### 5.1 Bit Ordering

Bits are sent on the PWI MSB first. In the following pictures, bits and frames are shown such that both individual bits and frames are represented, in left-to-right reading order, as they would transfer across the interface.

### 5.2 Frame Structure

Each command/data frame on the PWI consists of a start bit ('1'), two reserved bits ('00'), 8 payload bits and a stop bit ('0'). According to the contents of the payload bits different kinds of frame types can be defined: Core voltage adjustment frame, command frame and data frame. The figure below shows the basic frame structure.



**Figure 5-1. Basic Frame Structure**

A PWI slave identifies frame types based on their relative position and content. A new incoming frame is always interpreted to be either a core voltage adjustment frame or a command frame. Payload bit 7 is used to separate the two. Therefore this bit is also called the V/C (Voltage / Command) bit.

Data frames appear only in association with a preceding command frame. PWI slave only sends data frames in response to PWI master commands.

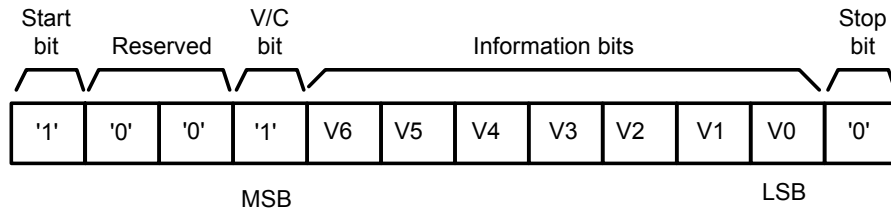
#### 5.2.1 No Response Frame

A No Response Frame is a frame that contains only zeroes. Even the start bit is logic zero. This frame is generated by driving SPWI to '0' for the entire duration of the frame.

The PWI slave responds with this frame when PWI master tries to read an unsupported register. The PWI slave responds with this frame when the PWI master attempts to authenticate and the slave does not support a specific authentication. See section 5.2.7 for information on authentication.

## 5.2.2 Core Voltage Adjustment Frame

In a Core Voltage Adjustment Frame the first payload bit (V/C) is '1'. The 7 remaining payload bits carry the voltage value. See the next figure for an example.



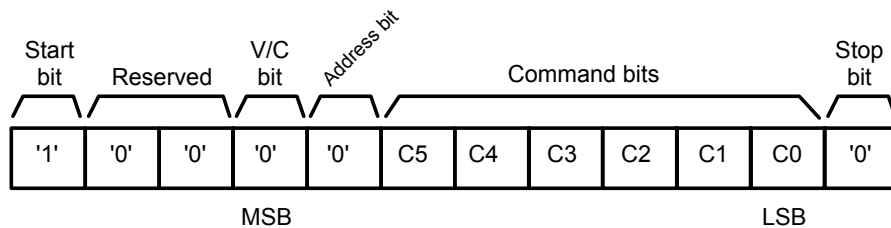
**Figure 5-2. Core Voltage Adjust Frame**

See section 7.4 for information on voltage coding for this, or any other, command. Note that this frame has the same effect as executing a register write to register R0. See 5.2.5 for details on register write. The core voltage adjustment frame command is the preferred command for writing register R0 since the register write command takes twice as long to execute.

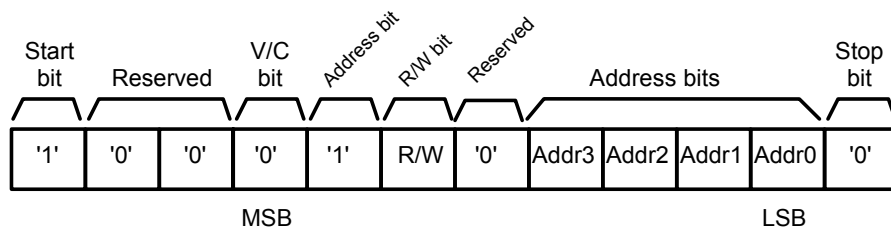
## 5.2.3 Command Frame

In Command Frame the first information bit (V/C) is '0'. The next bit (6) indicates if the command contains an address ('1') or not ('0'). If an address is present then payload bits [3:0] contain the address. If address is present then payload bit 5 indicates whether the operation is read ('1') or write ('0'). In read/write commands the payload bit 4 is always zero. It may be used in future to expand the address space to five bits.

If the command does not include an address then all remaining bits identify the command. See section 7.1 for the list of available commands.



**Figure 5-3. Command Frame without Address**



**Figure 5-4. Command Frame with Address**

### 5.2.4 Data Frame

Data frames have a start bit ('1'), the two reserved bits, 8 data bits (payload) and a stop bit ('0') at the end. Data frames do not occur independently, but are always associated with, or occur in response to, command frames.

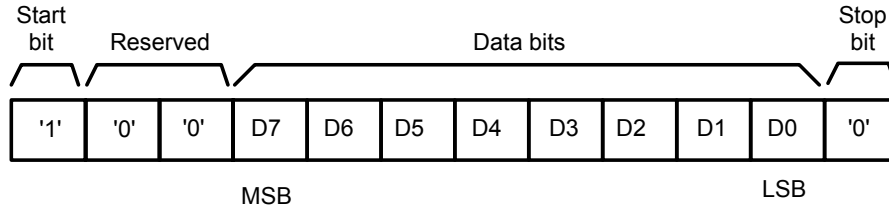


Figure 5-5. Data Frame

### 5.2.5 Write Sequence

The write sequence starts with a write command that contains the address to write to, followed by a data frame with the data to be written. Note that the data frame always immediately follows the command frame.

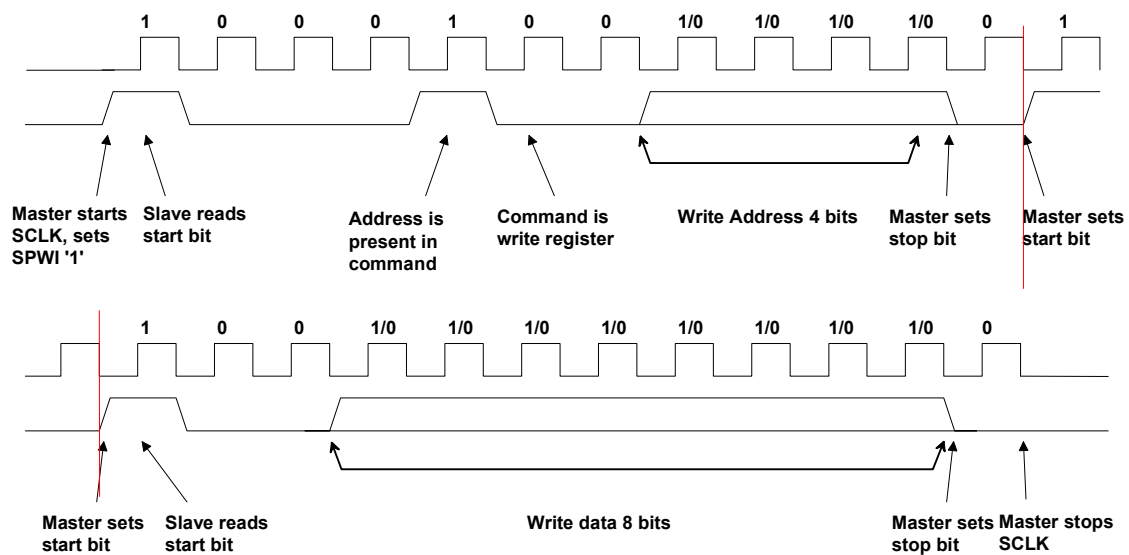
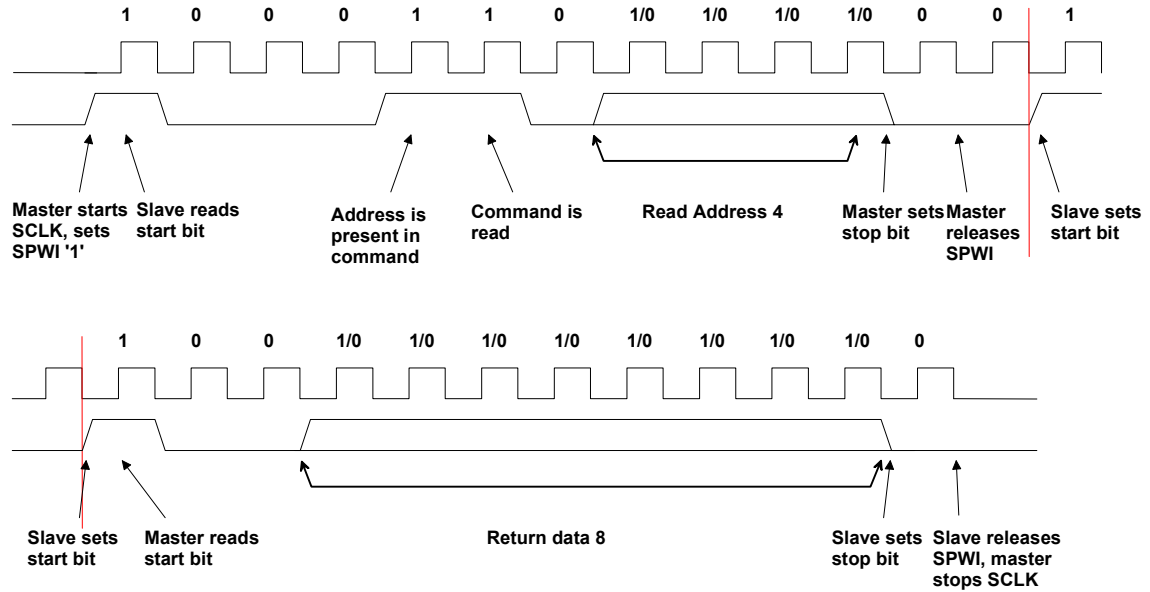


Figure 5-6. Register Write

### 5.2.6 Read Sequence

The read sequence starts with a read command, then a 1-clock cycle turn-around period, followed by the data frame sent from the slave. Note that the data frame always immediately follows the one clock period turn-around time.



**Figure 5-7. Register Read**

Note: The last falling SCLK edge of a read sequence and the assertion of the start bit on the SPWI by the master on any subsequent sequence may not occur at the same time. The PWI master must provide a turn-around time of at least one SCLK clock period. The PWI master does not generate clock transitions during this turn-around period.

### 5.2.7 Authentication Sequence

An authentication sequence is initiated by the PWI master as part of the SoC initialization. This sequence may be used to determine if the PMIC supports specific advanced power management techniques that may require licensing or for other vendor specific purposes. The data values for challenge frames and response frames are vendor specific.

Authentication sequence starts with the authenticate command, followed by the alternating challenge/response sequence. The PWI master transmits the challenge sequence using data frames. The data frames are interleaved with response frames, which are structurally data frames, from the slave.

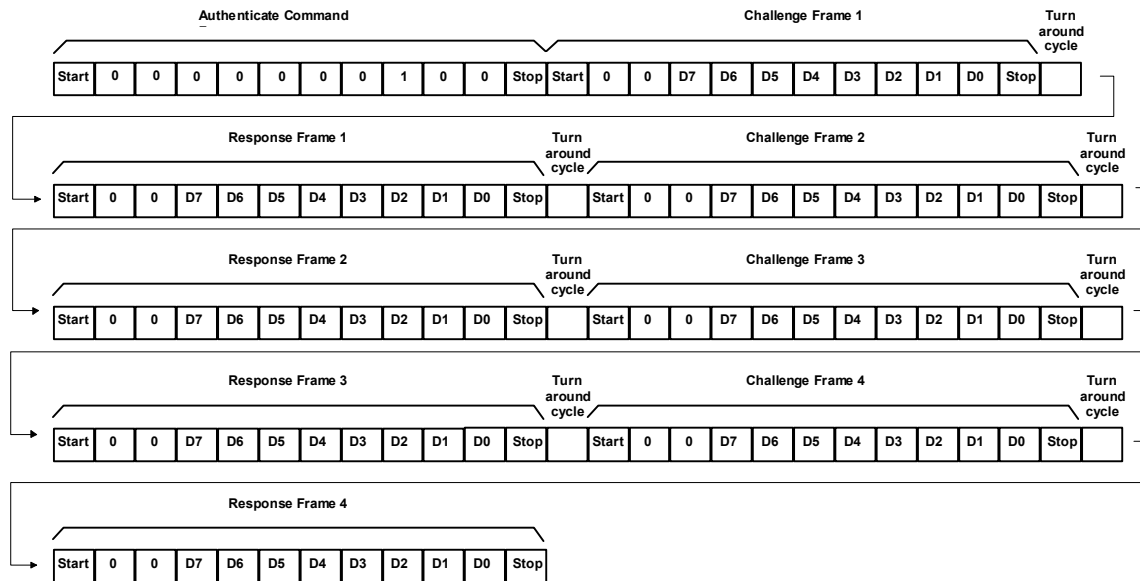


Figure 5-8. Authentication Sequence

## 6 PWI-Controlled Functions

### 6.1 Introduction

The PWI slave contains a register set of up to sixteen 8-bit registers. These registers control various voltage regulators and other functions inside a PWI compliant PMIC. Some of the registers are used to store information the PWI master can read in order to gain information of the status and operation of the PMIC.

### 6.2 Voltage Regulators

The primary function of a PWI compliant PMIC is to decode the incoming command frames and provide optimum voltages needed by the SoC.

It is mandatory for this PMIC to include a core voltage regulator and a PWI slave to control it. Other PWI slave voltage regulators are not mandatory and need not be implemented.

If a function is not used inside the PMIC, the corresponding control register in the PWI slave is also not used. Refer to Section 7 for a list of mandatory and optional functions inside the PWI slave.

#### 6.2.1 Core Voltage Regulator

The core voltage regulator is controlled by a 7-bit field in register R0. The output voltage is linearly controlled by the data word in the register between the minimum and maximum rated output voltage value of the regulator. See section 7.4 for further information on voltage coding.

The core voltage regulator is normally controlled with a dedicated command. The core voltage adjustment command provides a single frame write to register R0. This increases the available bandwidth on the PWI serial interface for core voltage adjustment.

#### 6.2.2 Memory Voltage Regulator

A PWI compliant PMIC may optionally include a regulator to control SoC memory supply voltage. The output voltage of this regulator is linearly controlled by a 7-bit field in register R1 in the PWI slave.

The PWI slave may optionally include a provision for allowing the core voltage and the memory voltage regulator output voltages to track each other.

#### 6.2.3 Memory Retention Voltage

Register R2 (See table 7.2) may be used to set memory supply voltage lower limit (retention level). If the regulator which is used to provide the supply voltage to the memories is programmed to a lower level than that indicated by R2, the memory supply voltage regulator output voltage is that indicated by R2.

In sleep mode the memory supply voltage is at the level indicated by register R2. The implementation of this function is optional.

### **6.2.4 N/P-well Voltage Regulators**

A PWI compliant PMIC optionally includes voltage regulators for controlling P-well (NMOS transistor) and/or N-well (PMOS transistor) bias voltages. These bias voltages are linearly controlled by the data in registers R5 and R6 in the PWI slave. See 7.4.6 and 7.4.7 for details.

### **6.2.5 Fixed Voltage Regulators**

A PWI compliant PMIC may optionally include one or more voltage regulators to provide fixed supply voltages to the SoC-circuit. These regulators are typically used to supply I/O-pads, PLLs, watchdog functions etc.

## **6.3 Other Functions**

### **6.3.1 Status Reporting**

A PWI compliant PMIC may include circuitry for generating information about the status of the various voltage regulators. Status information is contained in register R3 of the PWI slave. Register R3 is a mandatory register even if the circuitry is not implemented.

Refer to PWI register set in section 7.4 for further information.

### **6.3.2 User Defined Functions**

The PWI register set includes two optional registers, R9 and R10, for user defined device specific functions. Two bits in status register R3 are also reserved for user defined functions.

Refer to PWI register set in section 7.4 for further information.

## 7 PWI Slave Operation

### 7.1 Commands

A PWI slave must support the following 9 commands: Reset, Sleep, Shutdown, Wakeup, Core Voltage Adjust, Register Write, Register Read, Authenticate and Synchronize. Only the PWI master can issue commands. The PWI slave will only respond to the received commands using data frames. The following table summarizes all the commands:

**Table 7-1. Command Set**

Command	Voltage/Command Frame												
	Reserved			Payload									Stop bit
	Start bit	R1 bit	R0 bit	Bit 7 (Voltage / Command)	Bit 6 (Address present)	Bit 5 (Read / Write)	Bit 4 (Command 4)	Bit 3 (Command / address 3)	Bit 2 (Command / address 2)	Bit 1 (Command / address 1)	Bit 0 (Command / address 0)		
Core Voltage Adjust	1	0	0	1	V6	V5	V4	V3	V2	V1	V0	0	
Reset	1	0	0	0	0	0	1	0	0	0	0	0	
Sleep	1	0	0	0	0	0	1	0	0	0	1	0	
Shutdown	1	0	0	0	0	0	1	0	0	1	0	0	
Wakeup	1	0	0	0	0	0	1	0	0	1	1	0	
Register Read	1	0	0	0	1	1	0	A3	A2	A1	A0	0	
Register Write	1	0	0	0	1	0	0	A3	A2	A1	A0	0	
Authenticate	1	0	0	0	0	0	0	0	1	0	0	0	
Synchronize	1	1	1	1	1	1	1	1	1	1	1	0	

#### Notes

- Commands are always sent by the PWI master only.
- A Register Read-command is followed by a data frame from the slave after a bus turnaround cycle.
- A Register Write-command is followed by a data frame from the master immediately after the command.
- Authenticate command is followed by a sequence of data frame exchanges between the master and the slave. In this case these frame are called challenge and response frames.
- Any commands patterns not found above are ignored without error. They are treated as "no operation". (NOP).

### **7.1.1 Core Voltage Adjust**

The core voltage regulator output voltage is controlled with this command. The command allows transmission of a 7-bit voltage value in one frame. This single frame register write reduces the PWI bandwidth required for controlling the core voltage regulator.

The 7-bit voltage value contained in the command is written to a register controlling the regulator in the PWI slave.

### **7.1.2 Reset**

Writing the reset command will initialize the PWI slave and forces all registers to reset values (see table 7-2).

### **7.1.3 Sleep**

Writing the sleep command to the PWI slave activates the Sleep-mode. This will cause the logic core voltage to go to 0V, and the memory voltage will drop to its retention value. Other voltages retain their programmed values.

The sleep command does not alter any of the voltage control register values.

### **7.1.4 Shutdown**

This command will cause the PWI slave to switch off all regulators, thus causing all output voltages to go to zero. The PWI slave will go to the shutdown operating state and stay there.

Wake-up from shutdown mode is only possible with an external reset or by setting the external enable to zero and then back to '1'.

### **7.1.5 Wakeup**

This command allows the PWI slave to move from Sleep-state to Active-state. The voltage control registers contents, and therefore the regulator output voltages, are restored to their nominal, reset values.

### **7.1.6 Register Write**

Register write is a two-frame event consisting of the Register Write-command with a 4-bit register address included in the command, and a subsequent data frame that supplies the data to be written to the target register. See section 7.4 for details.

### 7.1.7 Register Read

Register read is a two-frame event consisting of the Register Read-command with the 4-bit register address included in the command. After the read command the PWI-master releases the SPWI line for the slave which then writes the contents of the target register out using a data frame format after one clock cycle bus turnaround period. The master supplies the clock signal for the entire operation.

Any read attempt by the PWI-master with an unsupported address results in a “No Response” frame from the PWI-slave.

### 7.1.8 Authenticate

Authenticate is a nine-frame event consisting of the Authenticate-command followed by four challenge/response frame sequences. An authentication sequence is initiated by the PWI master as part of the SoC initialization.

The PWI-slave must recognize the Authenticate-command and respond. If the slave does not support specific authentication then all response frames in the authentication sequence are of “No Response” type.

The full authentication sequence is described in section 5.2.7.

### 7.1.9 Synchronize

The PWI-slave interprets the commands coming from the master based on the data it sees in a frame. If for some reason the master and slave get out of sync with their frames then PWI communication is lost. This situation might arise during power-up sequences due to glitches on the SCLK line etc.

The Synchronize command enables recovery from such a situation. By sending a stream of ‘1’s the master can force the slave to resynchronize to the stop bit (‘0’) of the command. Because the command sequence is all ‘1’s, it is possible to detect this sequence even in an out-of-synchronization situation. The slave will assume that the first ‘0’ after 11 consecutive ‘1’s is the frame stop bit.

## 7.2 Operating States

The diagram below shows the four operating states that can be used to describe the operation of the voltage regulators controlled by the PWI-slave. The four operating states are: Active, Sleep, Shutdown and Startup. The states define the operation of the regulators under different conditions.

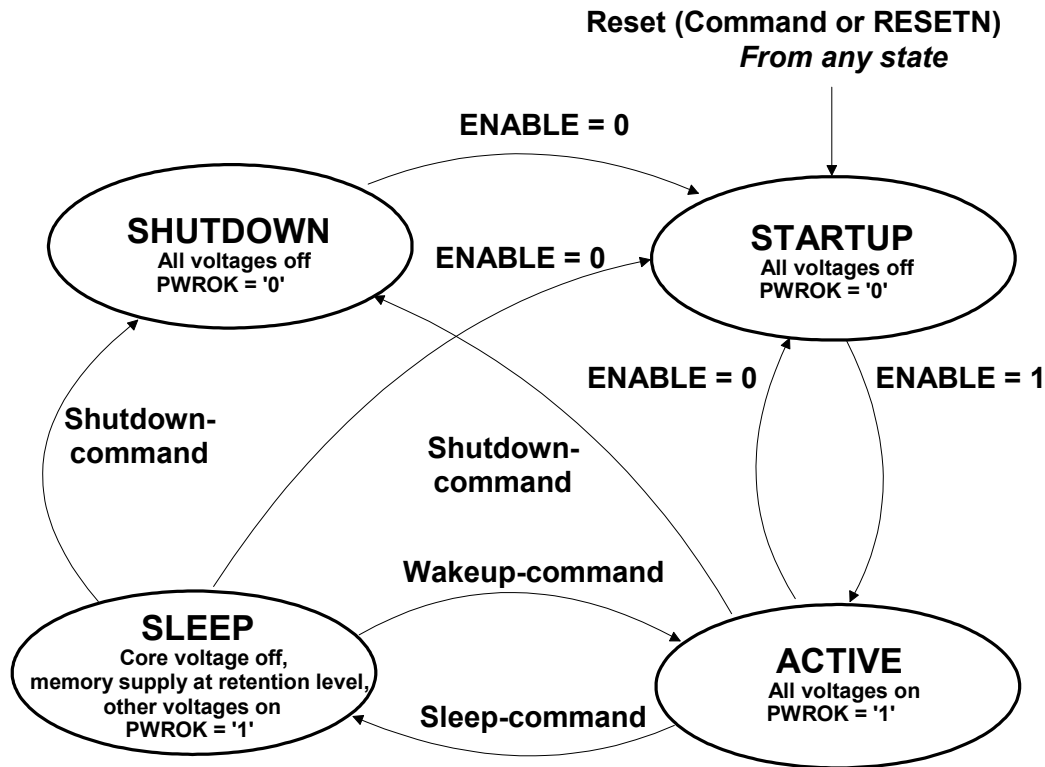


Figure 7-1. PWI Slave State Diagram

### 7.2.1 Startup

This state is the default state after a reset, and if the ENABLE-signal has been '0' in any state. All regulators are off in this state, and the PWROK-output is '0'. When the ENABLE-signal goes high the regulators power up and the system transitions to the Active state.

The power-up (or power-down) sequence of the regulators is device specific. The sequences in which voltage regulators activate, and the time required, depend on the needs of the target application and SoC.

## 7.2.2 Active

This is the normal operating state of the regulator system after the power-on sequence. Immediately after the power-on sequence all regulators' outputs are at their default levels. These levels are defined during device design. Core voltage is at its maximum value (top of the programming range). PWROK-output is '1'.

In Active-state the PWI master can control any of the voltages on the PMIC by programming the corresponding PWI registers.

## 7.2.3 Sleep

Sleep state is initiated using the Sleep-command in the Active state. In this state the core logic supply voltage is 0V irrespective of the value in the core voltage control register.

The memory supply voltage is at its retention level, which can be controlled using the memory retention voltage register R2. If memory retention voltage register is not implemented then memory supply voltage will zero.

Fixed voltage regulators, if implemented, are at their programmed levels. PWROK-output is '1'.

It is possible to program any of the PWI slave registers during sleep.

A wakeup-command returns the PWI-slave to the Active state. The voltage control registers contents, and therefore the regulator output voltages, are restored to their nominal, reset values. A reset-command returns the PWI slave to the Startup state. If shutdown-command is received the device powers down and goes to the Shutdown state.

## 7.2.4 Shutdown

The PWI slave is in Shutdown state after a Shutdown-command is received while in either the Active or Sleep states. All output voltages are 0V. PWROK-output is '0'.

The device moves to the Startup state when ENABLE goes low or a reset is supplied.

# 7.3 PMIC External Control Signals

## 7.3.1 RESETN

External reset is an asynchronous asserted low signal. Setting RESETN low will cause the PMIC to go to the Startup-state. Voltage regulation is lost once RESETN is asserted.

## 7.3.2 ENABLE

ENABLE is an asynchronous active high signal. The PMIC will start its power-up sequence once the ENABLE-signal goes high in the Startup-state. If ENABLE signal goes low in any state the device will go to the Startup-state.

## 7.3.3 PWROK

PWROK, asserted high, indicates that the PWI controlled regulators on the PMIC have valid output voltages. PWROK-output is an active high asynchronous output that can be used to generate reset signals etc. for the SoC.

## 7.4 Register Set

The PWI standard supports sixteen 8-bit registers on the PWI slave. The following table summarizes these registers while the sub-sections, which follow, provide additional detail.

**Table 7-2. Register Summary**

Register Address	Register Name	Mandatory (Note 2)	Register Usage	Type	Reset Default Value (Note 1)								
					7	6	5	4	3	2	1	0	
0x0	R0	Y	Core voltage	R/W	0	1	1	1	1	1	1	1	1
0x1	R1	N	Memory voltage	R/W	0	*	*	*	*	*	*	*	*
0x2	R2	N	Memory retention voltage	R/W	0	*	*	*	*	*	*	*	*
0x3	R3	Y	Status register (Note 3)	R/O	0	0	*	*	0	0	0	0	0
0x4	R4	Y	PWI version number	R/O	0	0	0	0	0	0	0	0	1
0x5	R5	N	N-well voltage	R/W	0	0	0	0	0	0	0	0	0
0x6	R6	N	P-well voltage	R/W	0	0	0	0	0	0	0	0	0
0x7	R7	N	I/O voltage	R/W	0	*	*	*	*	*	*	*	*
0x8	R8	N	Fixed voltage	R/W	0	*	*	*	*	*	*	*	*
0x9	R9	N	User register 1	R/W	*	*	*	*	*	*	*	*	*
0xA	R10	N	User register 2	R/W	*	*	*	*	*	*	*	*	*
0xB	R11	N	Reserved	R/W	-	-	-	-	-	-	-	-	-
0xC	R12	N	Reserved	R/W	-	-	-	-	-	-	-	-	-
0xD	R13	N	Reserved	R/W	-	-	-	-	-	-	-	-	-
0xE	R14	N	Reserved	R/W	-	-	-	-	-	-	-	-	-
0xF	R15	N	Reserved for manufacturing	R/W	*	*	*	*	*	*	*	*	*

Note 1: Any reset default values marked with an \* are user defined.

Note 2: Any non-mandatory registers and the functions they provide are optional. If a function is not implemented then the corresponding register is not implemented either. Any read of a not implemented register should return a "no response" frame as detailed in section 5.2.1.

Note 3: The default values of R3 bits [3:0] depend on the presence of regulator output voltage monitoring circuitry. If such circuitry is present, the default value is '0'. Else it is '1'. See 7.4.4 for details.

### 7.4.1 R0 - Core Voltage Register

Address        0x0  
 Type            R/W  
 Reset Default  0x7F

Bit	Field Name	Description or Comment
7	Sign	This bit is fixed to '0'. Reading this bit will result in a '0'. Any data written into this bit position using the Register Write command is ignored.
6:0	Voltage	<p>Core voltage value.</p> <p>A code of all ones indicates maximum voltage while a code of all zero indicates minimum voltage. Voltage coding is linear. Absolute maximum and minimum levels are determined by the PMIC designer.</p> <p>The number of voltage bits implemented is flexible. The maximum voltage resolution is 7 bits while the minimum is 1 bit. The number of bits can be reduced by dropping LSB bits. If only one bit is used (bit 6) then this bit can act as an on/off control or a selector between maximum/minimum voltage levels.</p>

### 7.4.2 R1 - Memory Voltage Register

Address        0x1  
 Type            R/W  
 Reset Default  User defined

Bit	Field Name	Description or Comment
7	Sign	This bit is fixed to '0'. Reading this bit will result in a '0'. Any data written into this bit position using the Register Write command is ignored.
6:0	Voltage	<p>Memory voltage value. This is the supply voltage applied to on-chip memories. See section 7.2 for additional details.</p> <p>A code of all ones indicates maximum voltage while a code of all zero indicates minimum voltage. Voltage coding is linear. Absolute maximum and minimum levels are determined by the PMIC designer.</p> <p>The number of voltage bits implemented is flexible. The maximum voltage resolution is 7 bits while the minimum is 1 bit. The number of bits can be reduced by dropping LSB bits. If only one bit is used (bit 6) then this bit can act as an on/off control or a selector between maximum/minimum voltage levels.</p>

### 7.4.3 R2 - Memory Retention Voltage Register

Address        0x2  
 Type            R/W  
 Reset Default   User defined

Bit	Field Name	Description or Comment
7	Sign	This bit is fixed to '0'. Reading this bit will result in a '0'. Any data written into this bit position using the Register Write command is ignored.
6:0	Voltage	Memory retention voltage value. This is the memory voltage supplied to on-chip memories during Sleep state. See section 7.2 for additional details.  A code of all ones for bits 6:0 indicates maximum voltage while a code of all zero indicates minimum voltage. Voltage coding is linear. Absolute maximum and minimum levels are determined by the PMIC designer.

### 7.4.4 R3 - Status Register

Address        0x3  
 Type            Read Only  
 Reset Default   Implementation specific. See note 1 below.

Bit	Field Name	Description or Comment
7	Reserved	Reserved. Do not use. See note 1 and 3 below.
6	Reserved	Reserved. Do not use. See note 1 and 3 below.
5	User Bit	User defined function. See notes 1 and 2 below.
4	User Bit	User defined function. See notes 1 and 2 below.
3	Fixed OK	Fixed voltage regulator OK when set. See note 1 below.
2	IO OK	IO voltage regulator OK when set. See note 1 below.
1	Memory OK	Memory voltage regulator OK when set. See note 1 below.
0	Core OK	Core voltage regulator OK when set. See note 1 below.
<p>Note 1: Reset default values for this register.</p> <p>Bits 6,7: Reset to '0' – reserved status bits.</p> <p>Bits 4,5: Reset to '0' if unused; reset to User Defined Value if used.</p> <p>Bits 0,1,2,3: Reset to '1' if voltage regulator output valid flag is not implemented. Reset to '0' if such a flag is implemented for the corresponding regulator. After reset flag bit indicates whether the output voltage is within acceptable limits of the programmed voltage level ('1') or not ('0').</p>		
<p>Note 2: If a User Bit is unused reads should always return a zero.</p>		
<p>Note 3: Reserved bits always return zero on read.</p>		

### 7.4.5 R4 - PWI Version Number Register

Address        0x4  
 Type            Read Only  
 Reset Default  0x01

Bit	Field Name	Description or Comment
7:0	Version	PWI version number. At this point in time, the only valid version is 0x01.

### 7.4.6 R5 - N-Well Voltage Register

Address        0x5  
 Type            R/W  
 Reset Default  0x00

Bit	Field Name	Description or Comment
7	Sign	Sign bit. A zero indicates the voltage is above the reference while a one indicates the voltage is below the reference. Specifically, a zero with a voltage field of all ones indicates maximum absolute positive voltage difference compared to the reference while a one with a voltage field of all ones indicates maximum negative voltage difference compared to the reference. The sign bit is a "don't care" when the voltage field is zero, that is, the threshold voltage is equal to the reference.
6:0	Voltage	N-Well (PMOS transistors) voltage value. Referenced to core voltage. This field controls the bias voltage for threshold scaling.  A code of all ones indicates maximum voltage while a code of all zero indicates minimum voltage. Voltage coding is linear. Absolute maximum and minimum levels are determined by the PMIC designer.  The number of voltage bits implemented is flexible. The maximum voltage resolution is 6 bits while the minimum is 1 bit. The number of bits can be reduced by dropping LSB bits. If only one bit is used (bit 6) then this bit can act as an on/off control or a selector between maximum/minimum voltage levels.

### 7.4.7 R6 - P-Well Voltage Register

Address        0x6  
 Type            R/W  
 Reset Default  0x00

Bit	Field Name	Description or Comment
7	Sign	Sign bit. A zero indicates the voltage is above the reference while a one indicates the voltage is below the reference. Specifically, a zero with a voltage field of all ones indicates maximum absolute positive voltage difference compared to the reference while a one with a voltage field of all ones indicates maximum negative voltage difference compared to the reference. The sign bit is a “don’t care” when the voltage field is zero, that is, the threshold voltage is equal to the reference.
6:0	Voltage	<p>P-Well (NMOS transistors) voltage value. Referenced to core ground. This field controls the bias voltage for threshold scaling.</p> <p>A code of all ones indicates maximum voltage while a code of all zero indicates minimum voltage. Voltage coding is linear. Absolute maximum and minimum levels are determined by the PMIC designer.</p> <p>The number of voltage bits implemented is flexible. The maximum voltage resolution is 7 bits while the minimum is 1 bit. The number of bits can be reduced by dropping LSB bits. If only one bit is used (bit 6) then this bit can act as an on/off control or a selector between maximum/minimum voltage levels.</p>

### 7.4.8 R7 - I/O Voltage Register

Address        0x7  
 Type            R/W  
 Reset Default  User defined

Bit	Field Name	Description or Comment
7	Sign	This bit is fixed to '0'. Reading this bit will result in a '0'. Any data written into this bit position using the Register Write command is ignored.
6:0	Voltage	<p>IO voltage value. Normally used to control the IO supply regulator.</p> <p>A code of all ones indicates maximum voltage while a code of all zero indicates minimum voltage. Voltage coding is linear. Absolute maximum and minimum levels are determined by the PMIC designer.</p> <p>The number of voltage bits implemented is flexible. The maximum voltage resolution is 7 bits while the minimum is 1 bit. The number of bits can be reduced by dropping LSB bits. If only one bit is used (bit 6) then this bit can act as an on/off control or a selector between maximum/minimum voltage levels.</p>

### 7.4.9 R8 - Fixed Voltage Register

Address        0x8  
 Type            R/W  
 Reset Default   User defined

Bit	Field Name	Description or Comment
7	Sign	This bit is fixed to '0'. Reading this bit will result in a '0'. Any data written into this bit position using the Register Write command is ignored.
6:0	Voltage	Fixed voltage value. Normally used to control a fixed voltage supply regulator. For example, the PLL supply for a SoC.  A code of all ones indicates maximum voltage while a code of all zero indicates minimum voltage. Voltage coding is linear. Absolute maximum and minimum levels are determined by the PMIC designer.  The number of voltage bits implemented is flexible. The maximum voltage resolution is 7 bits while the minimum is 1 bit. The number of bits can be reduced by dropping LSB bits. If only one bit is used (bit 6) then this bit can act as an on/off control or a selector between maximum/minimum voltage levels.

### 7.4.10 R9 - User Register 1

Address        0x9  
 Type            R/W  
 Reset Default   User defined

Bit	Field Name	Description or Comment
7:0	User Defined	This register can be used for any function deemed necessary by the PMIC designer.

### 7.4.11 R10 - User Register 2

Address        0xA  
 Type            R/W  
 Reset Default   User defined

Bit	Field Name	Description or Comment
7:0	User Defined	This register can be used for any function deemed necessary by the PMIC designer.

**7.4.12 R11-R14 - Reserved Registers**

Address        0xB, 0xC, 0xD, 0xE  
 Type            R/W  
 Reset Default zero

Bit	Field Name	Description or Comment
7:0	Reserved	These registers are not implemented on PWI version one. Writes should be "don't care" and reads should always return a "No Response Frame."

**7.4.13 R15 - Manufacturing Register**

Address        0xF  
 Type            R/W  
 Reset Default User defined

Bit	Field Name	Description or Comment
7:0	User Defined	This register is reserved for test, debug and manufacturing purposes only. This register is not used during normal operation. The test, debug and manufacturing functions controlled through this register are defined by the PMIC designer.