Errata:

PowerWise™ Interface Specification

Revision 1.2

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ARM

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Errata Release Notes

This errata document is an addendum to the following released version of the PowerWise Interface Specification. Please check www.pwistandard.org for latest releases of the specification and the errata.

Revision	Issue Date	Comment
1.0	01 October 2003	Original release, PWI specification

Errata Revision History

Revision	Issue Date	Comment
1.0	15 June 2004	Original release - Section 5.2.6 clarification - Section 7.4.6 correction
1.1	30 June 2004	Linear control requirement for I/O voltage regulator and fixed voltage regulator removed: - Section 7.4.8 correction - Section 7.4.9 correction Registers R11-R13 are changed to user registers: - Table 7-2 change - Section 7.4.12 change and renumbering (→ 7.4.15) - Section 7.4.13 renumbering (→ 7.4.16) - New section 7.4.12 User Register 3 - New section 7.4.13 User Register 4 - New section 7.4.14 User Register 5
1.2	28 January 2005	SPWI data line setup and hold time specifications relaxed: - Section 4.4 change Authentication sequence end bus turn-around cycle explanation: - Section 5.2.7 addition Memory retention voltage limit impact in active mode is made optional to match 7.4.3: - Section 6.2.3 change PWI slave state diagram is corrected to refer only to the mandatory configuration changes for each state: - Section 7.2 correction Memory retention voltage register R2 bit width is made flexible by dropping LSB bits: - Section 7.4.3 correction Wakeup-command impact on other regulators than those controlled by R0 is made optional: - Section 7.1.5 change - Section 7.2.3 change

Chapter 4

Section 4.4 PWI Data-line (SPWI)

Background: The setup and hold time requirements in Table 4-1 Timing Parameters are unnecessarily tight considering the SCLK minimum pulse width of 26ns.

Change: The setup time specification in Table 4-1 is changed to 7 ns. Hold time specification is changed from 10 ns to 26 ns. The revised Table 4-1 is shown below:

Table 4-1. Timing Parameters

Symbol	Description	Value	Constraint type
T_D	Data valid time	18 ns	Maximum
T_S	Setup time	7 ns	Minimum
T_H	Hold time	26 ns	Minimum

Explanation: Relaxing the setup and hold time specifications allows for easier timing closure on the PWI 1.0 slave and master implementations.

Chapter 5

Section 5.2.6 Read Sequence

Background: The note after figure 5-7 on page 15 in section 5.2.6 can cause misunderstandings.

Change: After the note following figure 5-7 another note is inserted:" Note 2: During the bus turn-around period of the read sequence, after the register read command frame from the PWI master and before the data frame from the PWI slave, the PWI master provides a single clock pulse on the SCLK-line. This clock period starts when PWI master releases SPWI and ends when the PWI slave sets the start bit of the data frame."

Explanation: Two bus turn around periods are associated with the register read sequence: The first occurs after the register read command frame and before the data frame from slave, and another at the end of the register read sequence before another sequence is started.

The first turn-around period lasts one SCLK period and the master produces a single clock pulse during it. The second turn-around period lasts also one SCLK clock period but the master does not produce a clock pulse during this period. Any new sequence from the master can be initiated after the last turn-around period has expired.

Figure 5-7 on page 15 correctly shows the first turn-around period between the command and data frames, but does not show explicitly the second turn-around period. The figure below shows the second situation. Please refer to figure 5-7 in PWI 1.0 specification for the complete register read sequence.

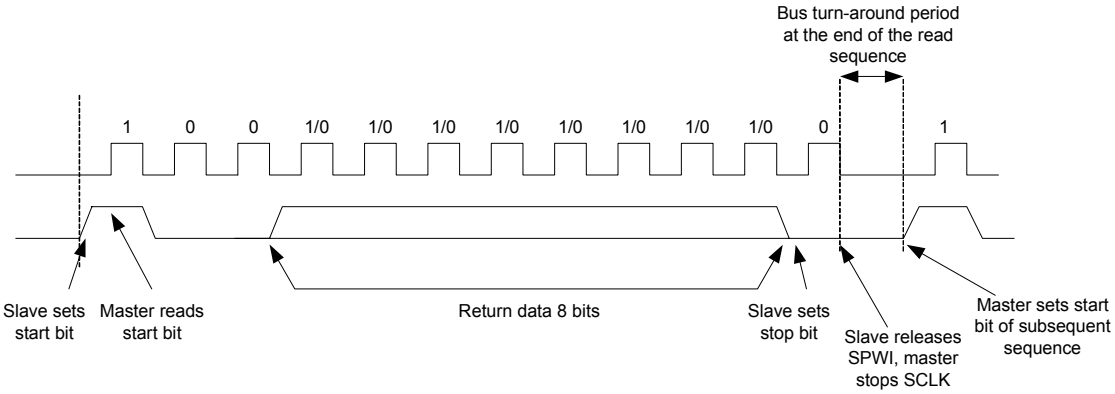

Figure 5-7. Bus turn-around at the end of a read sequence.

Section 5.2.7 Authentication Sequence

Background: The authentication sequence ends with a response frame from the PWI slave to the PWI master. Therefore there has to be a bus turn-around period after the authentication sequence before any subsequent frames on the PWI.

Change: The same comment about the turn-around period that is mentioned in section 5.2.6 Read Sequence is added to the end of section 5.2.7. The added paragraph reads:" There is a bus turn-around period after the end of the authentication sequence. This period lasts one SCLK clock period and the PWI master does not produce a clock pulse during this period."

Explanation: Every time there is a change in the direction of data transfer on the SPWI line a turn-around period has to occur to enable PWI master and slave to hand over SPWI line control. At the end of the authentication sequence the PWI slave that sent the last response frame will relinquish the SPWI line control to PWI master so that normal, master controlled, operation may resume. This is accomplished during the turn-around period. When a turn-around occurs at the end of an event there is no SCLK pulse associated with the turn-around period.

Chapter 6

Section 6.2.3 Memory Retention Voltage

Background: The clamping of memory supply voltage to lower limit stored in register R2 is made optional in Active-state.

Change: After the change the first paragraph of section 6.2.3 reads: “Register R2 (See table 7.2) may be used to set memory supply voltage lower limit (retention level). The regulator which is used to provide the supply voltage to the memories may be clamped to a voltage level indicated by R2 if the memory supply voltage regulator output voltage is programmed below that value.”

Explanation: The clamping of memory supply voltage to minimum value indicated by R2 is made optional to support SoC designs which do not use level shifters in the SoC core – memory interface. It is still allowed to implement a clamping function if the application needs it.

There is no change to memory retention register operation in Sleep-mode.

Chapter 7

Section 7.1.5 Wakeup

Background: The requirement of Wakeup-command resetting all voltage regulators to nominal values upon wakeup-event is removed. Only the core voltage regulator is required to reset to nominal value after wakeup.

Change: After the change the section 7.1.5 reads:" This command allows the PWI slave to move from Sleep-state to Active-state. The voltage control register R0 is set to nominal value. Therefore the core voltage regulator output voltage is restored to its nominal, reset value.

Other PWI 1.0 slave registers, except for R3[3:0] and R4, may be reset or left unaffected by the wakeup-command based on the device manufacturers preference. Register bits R3[3:0] are controlled by voltage monitoring circuitry or are '1111' (see sections 6.3.1 and 7.4.4). R4 is fixed."

Explanation: The earlier requirement of having to reset all regulators to nominal voltages was too restrictive as it limited device manufacturers options of implementing optimal behavior for the target application, especially in the user registers. This change removes those restrictions allowing for more flexible implementations.

Section 7.2 Operating States

Background: The operating state diagram (Figure 7-1.) gives an impression that all voltage regulators have to be on in the active state. However, the PWI specification dictates only the behavior of the core voltage regulator and to some degree the memory voltage regulator (see section 7.2.3 Sleep). Any user registers and / or optional voltage registers controlled by the PWI1.0 may have default voltages that are defined by device manufacturer. The enabling and disabling of optional regulators and user functions upon start-up is defined by device manufacturer.

Change: The updated PWI state diagram is shown below.

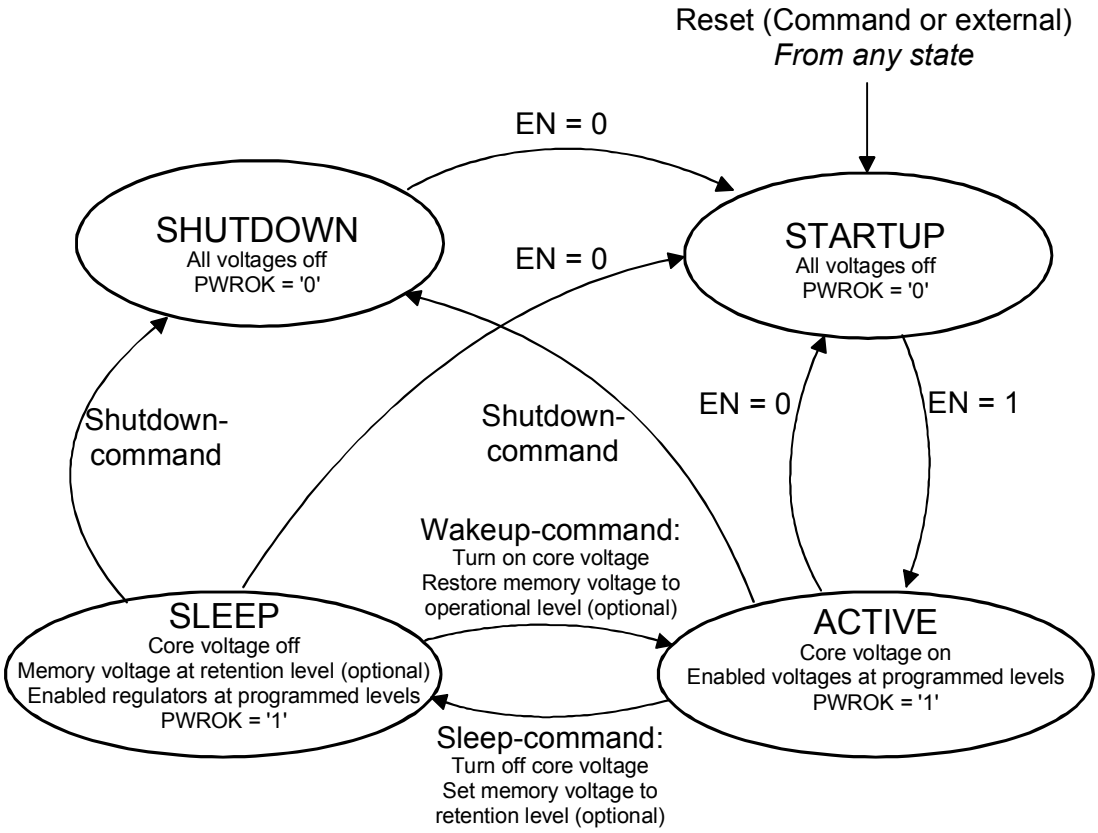

Figure 7-1. PWI Slave State Diagram

Explanation: Figure 7-1. PWI Slave State Diagram is updated to reflect explicitly those core voltage regulator configuration changes that are mandatory per PWI 1.0 specification. The implementation of a memory voltage regulator and retention voltage are optional EMU features as explained in sections 6.2.2 and 6.2.3 of the PowerWise Interface Specification. The state description text for each state and for Sleep- and Wakeup-commands is updated accordingly.

Section 7.2.3 Sleep

Background: The requirement of Wakeup-command resetting all voltage regulators to nominal values upon wakeup-event is removed. Only core voltage regulator and memory regulator are required to reset to nominal values after wakeup.

Change: After the change the last paragraph of section 7.2.3 reads:" A wakeup-command returns the PWI-slave to the Active state. The contents of register R0, and therefore the core voltage regulator output voltage, are restored to nominal, reset value. Other register values may be affected as well (see 7.1.5). A reset-command returns the PWI slave to the Startup state. If shutdown-command is received the device powers down and goes to the Shutdown state."

Explanation: The text change in 7.2.3 is necessary to align this section with the change in 7.1.5.

Section 7.4 Register Set

Background: PWI 1.0 registers R11-R13 are changed to User Registers like R9 and R10 are.

Change: Table 7-2 is updated. The updated table 7-2 is shown below.

Table 7-2. Register Summary

Register Address	Register Name	Mandatory (Note 2)	Register Usage	Type	Reset Default Value (Note 1)							
					7	6	5	4	3	2	1	0
0x0	R0	Y	Core voltage	R/W	0	1	1	1	1	1	1	1
0x1	R1	N	Memory voltage	R/W	0	*	*	*	*	*	*	*
0x2	R2	N	Memory retention voltage	R/W	0	*	*	*	*	*	*	*
0x3	R3	Y	Status register (Note 3)	R/O	0	0	*	*	0	0	0	0
0x4	R4	Y	PWI version number	R/O	0	0	0	0	0	0	0	1
0x5	R5	N	N-well voltage	R/W	0	0	0	0	0	0	0	0
0x6	R6	N	P-well voltage	R/W	0	0	0	0	0	0	0	0
0x7	R7	N	I/O voltage	R/W	0	*	*	*	*	*	*	*
0x8	R8	N	Fixed voltage	R/W	0	*	*	*	*	*	*	*
0x9	R9	N	User register 1	R/W	*	*	*	*	*	*	*	*
0xA	R10	N	User register 2	R/W	*	*	*	*	*	*	*	*
0xB	R11	N	User register 3	R/W	*	*	*	*	*	*	*	*
0xC	R12	N	User register 4	R/W	*	*	*	*	*	*	*	*
0xD	R13	N	User register 5	R/W	*	*	*	*	*	*	*	*
0xE	R14	N	Reserved	R/W	-	-	-	-	-	-	-	-
0xF	R15	N	Reserved for manufacturing	R/W	*	*	*	*	*	*	*	*

Explanation: Changing registers R11-R13 into User Registers allows more flexibility in implementing PWI 1.0 compliant devices.

Section 7.4.3 R2- Memory Retention Voltage Register

Background: The bit length of this register is made optional just like for registers R1 and R5-R13.

Change: A new paragraph of text is added to the “Description or Comment” column for bits 6:0 of register R2. The revised table in section 7.4.3 is shown below:

Bit	Field Name	Description or Comment
7	Sign	This bit is fixed to ‘0’. Reading this bit will result in a ‘0’. Any data written into this bit position using the Register Write command is ignored.
6:0	Voltage	Memory retention voltage value. This is the memory voltage supplied to on-chip memories during Sleep state. See section 7.3 for

		to on-chip memories during Sleep state. See section 7.2 for additional details. A code of all ones for bits 6:0 indicates maximum voltage while a code of all zero indicates minimum voltage. Voltage coding is linear. Absolute maximum and minimum levels are determined by the PMIC designer. The number of voltage bits implemented is flexible. The maximum voltage resolution is 7 bits while the minimum is 1 bit. The number of bits can be reduced by dropping LSB bits. If only one bit is used (bit 6) then this bit can act as an on/off control or a selector between maximum/minimum voltage levels.

Explanation: The permission to vary register R2 bit width was omitted from original revision of PWI 1.0 Standard and is now corrected.

Section 7.4.6 R5 - N-Well Voltage Register

Background: The description of the voltage value field for PWI register R5 contains an error in section 7.4.6 on page 27.

Change: The third paragraph of the description or comment for the voltage field of register R5 should read:" The number of voltage bits implemented is flexible. The maximum voltage resolution is 7 bits while minimum is 1 bit. The number of bits can be reduced by dropping LSB bits. If only one bit is used (bit 6) then this bit can act as an on/off switch or selector between maximum/minimum voltage levels."

Explanation: The earlier description or comment text incorrectly stated that the maximum voltage resolution would be 6 bits when R5 bits [6:0] are used for voltage control. The correct maximum resolution is 7 bits.

Section 7.4.8 R7 - I/O Voltage Register

Background: I/O voltage regulator voltage programming is not required to be linear. Device designer may code voltage values for the regulator as deemed appropriate.

Change: The second paragraph of the "Description or Comment"-field describing the use of R7 bits [6:0] is should read:" A code of all ones indicates maximum voltage while a code of all zero indicates minimum voltage. Absolute voltage levels and coding for intermediate voltage levels is defined by the PMIC designer."

Explanation: The earlier text indicated a requirement for linear control of the I/O voltage regulator. This is not indicated by Section 6.2.5. This change brings sections 6.2.5 and 7.4.8 into alignment.

Section 7.4.9 R8 - Fixed Voltage Register

Background: Fixed voltage regulator voltage programming is not required to be linear. Device designer may code voltage values for the regulator as deemed appropriate.

Change: The second paragraph of the “Description or Comment”-field describing the use of R8 bits [6:0] is should read:” A code of all ones indicates maximum voltage while a code of all zero indicates minimum voltage. Absolute voltage levels and coding for intermediate voltage levels is defined by the PMIC designer.”

Explanation: The earlier text indicated a requirement for linear control of the I/O voltage regulator. This is not indicated by Section 6.2.5. This change brings sections 6.2.5 and 7.4.9 into alignment.

Section 7.4.12 R11-R14 - Reserved Registers

Background: Sections need to be renumbered to accommodate new sections in chapter 7 due to added user registers.

Change: Section 7.4.12 is renumbered into section 7.4.15. Section 7.4.15 title is: “R14 Reserved Register”. New section contents are shown below:

Address 0xE
Type R/W
Reset Default zero

Bit	Field Name	Description or Comment
7:0	Reserved	This register is not implemented on PWI version 1.0. Writes should be “don’t care” and reads should always return a “No Response Frame.”

Explanation: Changing registers R11-R13 into User Registers allows more flexibility in implementing PWI 1.0 compliant devices.

Section 7.4.13 R15 – Manufacturing Register

Background: Sections need to be renumbered to accommodate new sections in chapter 7 due to added user registers.

Change: Section 7.4.13 is renumbered into section 7.4.16. No changes are made into the title or contents of this section.

Explanation: Changing registers R11-R13 into User Registers allows more flexibility in implementing PWI 1.0 compliant devices.

Chapter 7 New Sections

Three new sections are added into chapter 7. Sections added are 7.4.12, 7.4.13 and 7.4.14. The earlier sections 7.4.12 and 7.4.13 become 7.4.15 and 7.4.16 respectively with the changes indicated on page 11 of this document.

Section 7.4.12 R11 – User Register 3

Background: PWI 1.0 registers R11-R13 are changed into User Registers like R9 and R10 are.

Change: A new section titled “R11 – User Register 3” is added. The contents of this section are:

Address 0xB
Type R/W
Reset Default User defined

Bit	Field Name	Description or Comment
7:0	User Defined	This register can be used for any function deemed necessary by the PMIC designer.

Explanation: Changing registers R11-R13 into User Registers allows more flexibility in implementing PWI 1.0 compliant devices.

Section 7.4.13 R12 – User Register 4

Background: PWI 1.0 registers R11-R13 are changed into User Registers like R9 and R10 are.

Change: A new section titled “R12 – User Register 4” is added. The contents of this section are:

Address 0xC
Type R/W
Reset Default User defined

Bit	Field Name	Description or Comment
7:0	User Defined	This register can be used for any function deemed necessary by the PMIC designer.

Explanation: Changing registers R11-R13 into User Registers allows more flexibility in implementing PWI 1.0 compliant devices.

Section 7.4.14 R13 – User Register 5

Background: PWI 1.0 registers R11-R13 are changed into User Registers like R9 and R10 are.

Change: A new section titled “R13 – User Register 5” is added. The contents of this section are:

Address 0xD
Type R/W
Reset Default User defined

Bit	Field Name	Description or Comment
7:0	User Defined	This register can be used for any function deemed necessary by the PMIC designer.

Explanation: Changing registers R11-R13 into User Registers allows more flexibility in implementing PWI 1.0 compliant devices.

